

CLAIMS:

1. A data processing system, comprising a memory means (SDRAM) and a plurality of data processing means (IP) provided for accessing to said memory means (SDRAM), characterized by a communication interface means coupled between said memory means (SDRAM) and said plurality of data processing means (IP), said communication
5 interface means including a network of nodes (H_{11} , H_{12} , H_2), each node comprising at least one slave port (s) for receiving a memory access request from a data processing means (IP) or from a previous node and at least one master port (m) for issuing a memory access request to a next node or to said memory means (SDRAM) in accordance with the memory access request received at said slave port (s), wherein said at least one slave port (s) is connected to
10 a master port (m) of a previous node or to one of said data processing means (IP) and said at least one master port (m) is connected to a slave port (s) of a next node or to said memory means (SDRAM).
2. The data processing system according to claim 1, characterized in that at each
15 node means the number of said slave ports (s) is higher than the number of said master ports (m).
3. The data processing system according to claim 1 or 2, characterized in that said network of node means (H_{11} , H_{12} , H_2) is hierarchically structured.
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4. The data processing system according to claim 3, characterized in that said plurality of node means (H_{11} , H_{12} , H_2) are arranged in a directed acyclic graph structure.
5. The data processing system according to claim 4, characterized in that said
25 plurality of node means (H_{11} , H_{12} , H_2) are arranged in a tree structure.
6. The data processing system according to at least any one of the preceding claims, characterized in that said plurality of node means (H_{11} , H_{12} , H_2) include n groups of node means with $n \geq 2$, wherein each of the slave ports (s) of the node means (H_{11}) of a first

group is connected to one of said plurality of data processing means (IP), the master ports (m) of the node means (H_2) of the n^{th} group are coupled to said memory means (SDRAM), and each of the slave ports (s) of the node means (H_2) of the n^{th} group is connected to a master port (m) of the node means (H_{11}) of the $(n-1)^{\text{th}}$ group.

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7. The data processing system according to at least any one of the preceding claims, characterized in that said node means (H_{11} , H_{12} , H_2) are hubs.

8. The data processing system according to at least any one of the preceding claims, characterized in that said communication interface means further includes at least one local memory unit (MEM) adapted to be selectively accessed to by a memory access request.

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9. The data processing system according to claim 8, characterized in that at least one node means (H_{11} , H_{12} , H_2) further comprises at least one memory port (mp) to which a local memory unit (MEM) is connected.

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10. The data processing system according to claim 8 or 9, characterized in that said communication interface means includes a cache controller means for controlling at least a section of the local memory unit(s) (MEM) as a cache memory.

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11. The data processing system according to at least any one of the preceding claims, characterized in that said communication interface means further includes at least one synchronization means for streaming communication between data processing means (IP).

12. The data processing system according to claim 11, characterized in that at least one node means (H_{11} , H_{12} , H_2) includes said synchronization means for streaming communication between the data processing means (IP) directly or indirectly coupled to said node means.

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13. The data processing system according to claim 8 as well as to claim 11 or 12, characterized in that the local memory unit(s) (MEM) is (are) configured to provide the storage means for a first-in/first-out function and said synchronization means comprises a first-in/first-out administration means for controlling said local memory unit(s) (MEM).

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14. The data processing system according to at least any one of the preceding claims, characterized in that said communication interface means is provided on a single chip (C).
- 5 15. The data processing system according to claim 14, characterized in that at least a part of said plurality of data processing means (IP) is additionally provided on said single chip (C).